

c A-2  
EM  
6 8. (Amended) An anti-jitter circuit as claimed in claim 2 <sup>further</sup> including a monostable circuit connected to the output of said means for comparing.

A-3 Sub 85  
12. (Amended) An anti-jitter circuit as claimed in claim 8 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. (Amended) An anti-jitter circuit as claimed in claim 1 including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

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Sub 23  
D1  
14. (Amended) An anti-jitter circuit as claim in claim 1 <sup>further</sup> including means for maintaining the charge value of the charge packets substantially constant.

A-4  
Sub D1  
11 19. (Amended) An anti-jitter circuit as claimed in claim 2 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

Sub D1  
C/A-15  
15 21. (Amended) An anti-jitter circuit as claimed in claim 19 wherein said further negative feedback path comprises a low pass filter.

AL  
Sub D1  
17 23. (Amended) An anti-jitter circuit as claimed in claim 2 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c. voltage level as a switching level of said inverted gate means.

Sub D1  
19 25. (Amended) An anti-jitter circuit as claimed in claim 2 including means providing a low impedance path between the input and the output of the negative feedback path.

Cancel claim 28 without prejudice.

• Please add the following new claims 29-30:

Sub D1  
13 29. (New) An anti-jitter circuit as claimed in claim 20 wherein said further negative feedback path comprises a low pass filter.

Sub B7  
30. (New) An anti-jitter circuit as claimed in claim 29 wherein said low pass filter comprises the combination of a resistor and a capacitor.